



Product Information

Product Categories

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UDA1380; Stereo audio coder-decoder for MD, CD and MP3

Information as of 2004-03-16

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General description

The UDA1380 is a stereo audio coder-decoder, available in TSSOP32 (UDA1380TT) and HVQFN32 (UDA1380HN) packages. All functions and features are identical for both package versions. The term 'UDA1380' in this document refers to both UDA1380TT and UDA1380HN, unless particularly specified.

The front-end of the UDA1380 is equipped with a stereo line input, which has a PGA control, and a mono microphone input with an LNA and a VGA. The digital decimation filter is equipped with an AGC which can be used in case of voice-recording.

The DAC part is equipped with a stereo line output and a headphone driver output. The headphone driver is capable of driving a 16 Ohm load. The headphone driver is also capable of driving a headphone without the need for external DC decoupling capacitors, since the headphone can be connected to a pin $V_{REF(HP)}$ on the chip.

In addition, there is a built-in short-circuit protection for the headphone driver output which, in case of short-circuit, limits the current through the operational amplifiers and signals the event via its L3-bus or I²C-bus register.

The UDA1380 also supports an application mode in which the coder-decoder itself is not running, but an analog signal, for instance coming from an FM tuner, can be controlled in gain and applied to the output via the headphone driver and line outputs.

The UDA1380 supports the I²S-bus data format with word lengths of up to 24 bits, the MSB-justified data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 18, 20 or 24 bits (LSB-justified 24 bits is only supported for the output interface).

The UDA1380 has sound processing features in playback mode, de-emphasis, volume, mute, bass boost and treble which can be controlled by the L3-bus or I²C-bus interface.

Features

1.1 General

- 2.4 to 3.6 V power supply
- 5 V tolerant digital inputs (at 2.7 to 3.6 V power supply)
- 24-bit data path for Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC)
- Selectable control via L3-bus microcontroller interface or I²C-bus interface; choice of 2 device addresses in L3-bus and I²C-bus mode
- **Remark:** This device does not have a static mode.
- Supports sample frequencies from 8 to 55 kHz for the ADC part, and 8 to 100 kHz for the DAC part. The ADC does not support DVD audio (96 kHz audio), only Mini-Disc (MD), Compact-Disc (CD) and Moving Picture Experts Group Layer-3 Audio (MP3). For playback 8 to 100 kHz is specified. DVD playback is supported
- Power management unit:
 - Separate power control for ADC, Automatic Volume Control (AVC), DAC, Phase Locked Loop (PLL) and headphone driver
 - Analog blocks like ADC and Programmable Gain Amplifier (PGA) have a block to power-down the bias circuits
 - When ADC and/or DAC are powered-down, the clocks to these blocks are also stopped to save power.
- **Remark:** By default, when the IC is powered-up, the complete chip will be in the Power-down mode.
- ADC part and DAC part can run at different frequencies, either system clock or Word Select PLL (WSPLL)
- ADC and PGA plus integrated high-pass filter to cancel DC offset
- The decimation filter is equipped with a digital Automatic Gain Control (AGC)
- Mono microphone input with Low Noise Amplifier (LNA) of 29 dB fixed gain and Variable Gain Amplifier (VGA) from 0 to 30 dB in steps of 2 dB
- Integrated digital filter plus DAC

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- Separate single-ended line output and one stereo headphone output, capable of driving a 16 Ohm load. The headphone driver has a built-in short-circuit protection with status bits which can be read out from the L3-bus or I²C-bus interface
- Digital silence detection in the interpolator (playback) with read-out status via L3-bus or I²C-bus interface
- Easy application.

1.2 Multiple format data input interface

- Slave BCK and WS signals
- I²S-bus format
- MSB-justified format compatible
- LSB-justified format compatible.

1.3 Multiple format data output interface

- Select option for digital output interface: either the decimator output (ADC signal) or the output signal of the digital mixer which is in the interpolator DSP
- Selectable master or slave BCK and WS signals for digital ADC output
Remark: SYSCLK must be applied in WSPLL mode and master mode
- I²S-bus format
- MSB-justified format compatible
- LSB-justified format compatible.

1.4 ADC front-end features

- ADC plus decimator can run at either WSPLL, regenerating the clock from WSI signal, or on SYSCLK
- Stereo line input with PGA: gain range from 0 to 24 dB in steps of 3 dB
- LNA with 29 dB fixed gain for mono microphone input, including VGA with gain from 0 to 30 dB in steps of 2 dB
- Digital left and right independent volume control and mute from +24 to -63.5 dB in steps of 0.5 dB.

1.5 DAC features

- DAC plus interpolator can run at either WSPLL (regenerating the clock from WSI) or at SYSCLK
- Separate digital logarithmic volume control for left and right channels via L3-bus or I²C-bus from 0 to -78 dB in steps of 0.25 dB
- Digital tone control, bass boost and treble via L3-bus or I²C-bus interface
- Digital de-emphasis for sample frequencies of: 32, 44.1, 48 and 96 kHz via L3-bus or I²C-bus interface
- Cosine roll-off soft mute function
- Output signal polarity control via L3-bus or I²C-bus interface
- Digital mixer for mixing ADC output signal and digital serial input signal, if they run at the same sampling frequency.

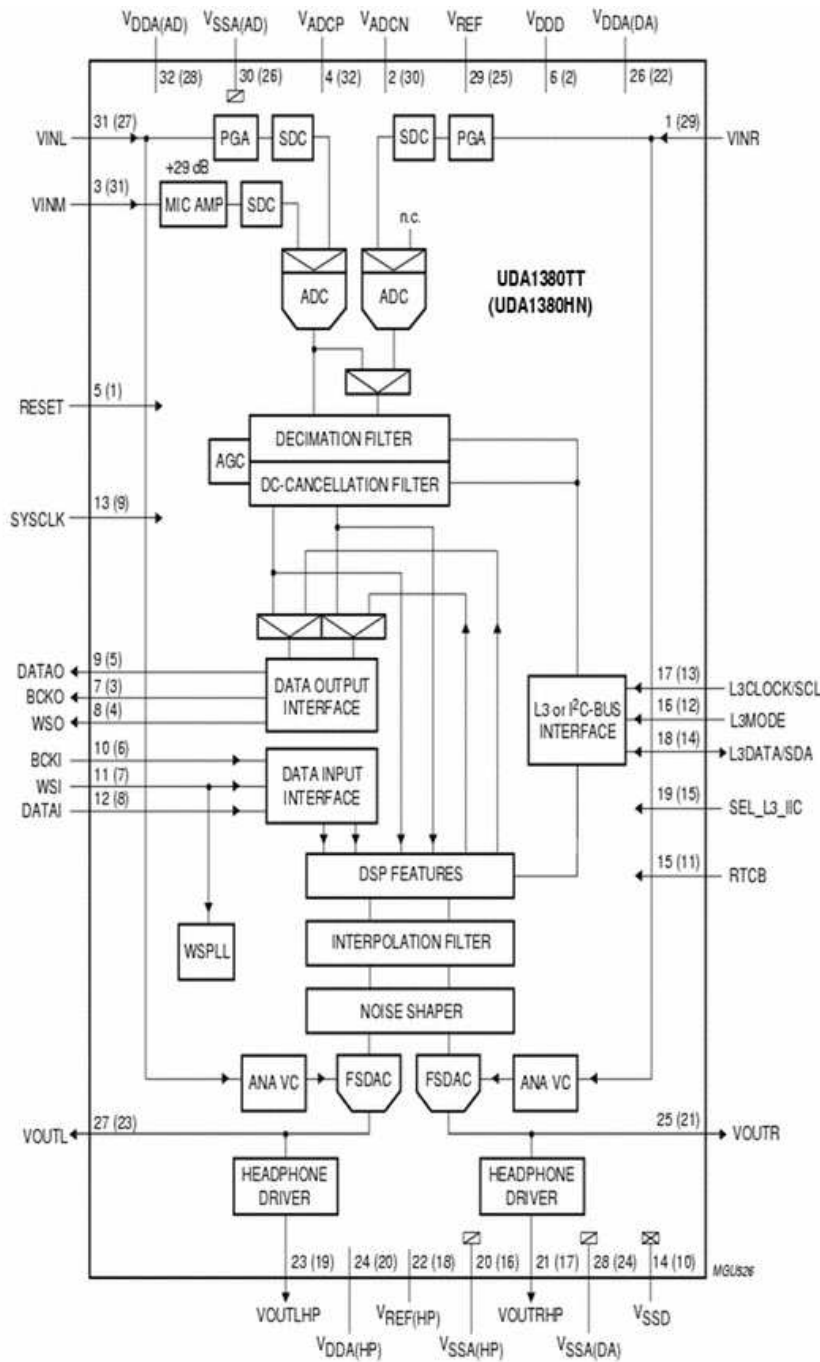
▣ Applications

This audio coder-decoder is suitable for home and portable applications like MD, CD and MP3 players.

▣ Datasheet

Datasheet title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
UDA1380; Stereo audio coder-decoder for MD, CD and MP3	04-Apr-03	Product specification	68	296	Download

▣ Blockdiagram(s)



Products, packages, availability and ordering

Type number	North American type number	Ordering code (12NC)	Marking/Packing PDF IC packing info	Package	Product status	Buy online
UDA1380HN/N1		9352 708 59118	Standard Marking * Reel Pack, SMD, 13"	SOT617-1 (HVQFN32)	Full production	-
UDA1380TT/N1		9352 683 70112	Standard Marking * Tube	SOT487-1 (TSSOP32)	Full production	-
		9352 683 70118	Standard Marking * Reel Pack, SMD, 13"	SOT487-1 (TSSOP32)	Full production	-
UDA1380TT/N2		9352 706 59112	Standard Marking * Tube	SOT487	Samples available	-
		9352 706 59118	Standard Marking * Reel Pack, SMD, 13"	SOT487	Samples available	-

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category.

Support & tools

[PDF](#) [P9xC557Ex 8-bit 80C51 with up to 64 Kbytes of internal program memory, 5 I/O ports and 10-bit ADC](#)(date 2003-03-07)

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